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A 4×6.25-Gbs Serial Link Transmitter Core in 0.18-µm CMOS for high-speed front-end ASICs

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In this paper, a 4×6.25 Gbps serial link transmitter core has been designed for high-speed front-end ASICs. The transmitter core is implemented in a commercial 0.18 um CMOS technology. The core consists of a common PLL and four individual transmitter channels. Each channel contains a 2-stage 20:2 serializer, a 2-stage half-rate feed-forward equalizer and a clock manager circuit. A new architecture of the clock and data path is proposed, and the overall power consumption is reduced by 40% compared with previous works. At a data rate of 6.25 Gbps, the simulation results show that the PLL and transmitter feature a phase jitter of 1.3 ps RMS and 11.2 ps pk-pk respectively. The 4-channel transmitter core occupies 0.44 mm2 and dissipates 27.7 mW/Gbps from 1.8 V supply. The chip is being packaged and will be tested soon in December.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

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